13.4 A 24mW 1.25Gb/s 13kΩ Transimpedance Amplifier Using Active Compensation

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The parasitic capacitance appearing at the input of a transimpedance amplifier (TIA) has been shown to have significant impacts on both the operating bandwidth and the noise characteristic of an optical receiver. The input capacitance is caused by the integrated photodiode (PD), the TIA, the bondpad, and the ESD protection circuit. To make the circuit more tolerant to large input capacitance, several design approaches focusing on achieving low input impedance, such as the multi-stage topology [1] and the regulated-cascode topology [2], have attracted a lot of attention in the past. However, the former design suffers from large power consumption and poor phase margin. The drawback of the latter design is the resulting poor noise characteristic. Recently, inductive-peaking techniques have been demonstrated to be very effective at extending the GBW of a TIA without obvious degradation in the noise characteristic [3, 4]. However, the limited inductance range in standard semiconductor processes makes them feasible only for ultra-high-speed applications. In contrast, the compensation technique using active circuit is more cost-effective and flexible. It is also capable of compensating both resistive and capacitive effects. In this paper, the feasibility of an active compensation technique for a TIA with enhanced GBW is demonstrated.

Figure 13.4.1 shows the proposed TIA circuit topology incorporating active compensation technique. The basic design concept is to cancel the loading effects caused by both the output impedance of the amplifier, Z_O, and the feedback resistance, R_F, by introducing a compensation element with effective impedance $-Z_C$. Hence, the closed-loop gain A_V can be significantly boosted. As a result, the input impedance is reduced and the operating bandwidth is extended. In general, both R_F and Z_O can be considered as resistive elements with parasitic capacitance. Therefore the compensation element has to provide both resistance and capacitance cancellation capabilities. Figure 13.4.1 also includes the circuit topology to implement the active compensation. The circuit consists of an inverting amplifier, A_C, 2 transistors, M_{C1} and M_{C2}, a loading capacitor C_{C1}, and the bias circuit. The desired negative resistance and negative capacitance are generated by M_{C1} and M_{C2} with the loading capacitor C_{C1}, respectively. The compensation strength can be adjusted by M_{C1} and C_{C1}.

Figure 13.4.2 shows the complete circuit diagram of the TIA IC. The IC is implemented in a standard 0.35μm CMOS technology. A common-source (CS) amplifier with a variable feedback resistor is used as the TIA core due to its excellent noise characteristic and phase margin. However, the low open-loop gain makes it difficult to achieve high transimpedance gain while a PD with large parasitic capacitance is used. The inverting amplifier of the compensation circuit is composed of M_1, M_2, M_3, R_1, R_2, and C_1. R_1 is used for dc level shift and C_1 is used as a decoupling capacitor. The gain of the inverting amplifier is proportional to the transconductance ratio of M_1 to M_2 and the phase shift is adjusted by R_2. The negative resistance is generated by M_4 and the negative capacitance is generated by the circuit including M_5, M_6, M_7, M_8. To achieve better capacitance matching to the CS amplifier, M_7 and M_8 are used as loading capacitors of M_5. In this design, the sizes of M_4 and M_5 are much smaller than that of M_{A1}. This guarantees minimum degradation in noise characteristic caused by the compensation circuit. Following the core circuit, a single-to-differential converter with automatic dc-cancellation and a CML output buffer capable of driving 50Ω loads are included. Figure 13.4.3 shows their circuit diagram. The lower cut-off frequency caused by the dc-cancellation circuit is around 50kHz.

For optical tests, the TIA IC is integrated with a commercial 1310nm InGaAs PIN PD in a chip-on-board assembly. The active area of the PD is 70μm in diameter. The reverse-bias voltage applied to the PD is slightly higher than 2V and its corresponding PD capacitance is around 0.7pF. The -3dB optical bandwidth is greater than 3GHz. The responsivity of the PD is 0.9A/W. Figure 13.4.4 shows the measured optical eye diagrams of the optical receiver at an input optical power of -27dBm under different compensation conditions. A 2^{31}-1 PRBS is used for the tests and the extinction ratio of the optical transmitter is 14dB. The results show a bandwidth enhancement factor of 3 achieved by the active compensation. Furthermore, there is no obvious degradation in noise characteristic observed in Figure 13.4.4 when the active compensation is enabled. Figure 13.4.5 shows the measured BER versus input optical power at 1.25Gb/s. The output signal of the optical receiver is amplified by a wideband post-amplifier before it is sent into the BER tester. At a BER of 10^{-12}, the measured sensitivity is about -29.5dBm. As the TIA IC is switched to its low-gain mode by applying 3V to the gate of the feedback transistor M_{A3}, the input overload optical power exceeds 0dBm. Figure 13.4.6 shows the measured optical eye diagrams at an input optical power of 0dBm.

The measured differential transimpedance gain is adjustable from 500Ω to 13kΩ without stability problem. The measured maximum differential output swing is $150mV_{PP}$. The complete TIA IC consumes 24mW from a 3V supply, the CS-TIA uses 12mW, and the active compensation circuit uses 3mW. The single-to-differential converter, the CML output buffer, and the bias circuit use 9mW in total. Figure 13.4.7 shows the die micrograph of the TIA IC. It occupies an area of 600×500μm² and the active area is about 200×100μm².

References:

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[4] C. H. Wu, et al., "CMOS Wideband Amplifiers Using Multiple Inductive-Series Peaking Technique," *IEEE J. Solid-State Circuits*, vol. 40, pp. 548-552, Feb., 2005.

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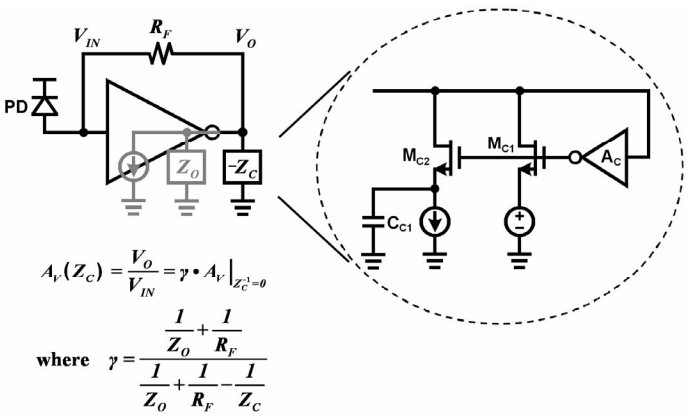

Figure 13.4.1: Circuit topology of TIA using active compensation.

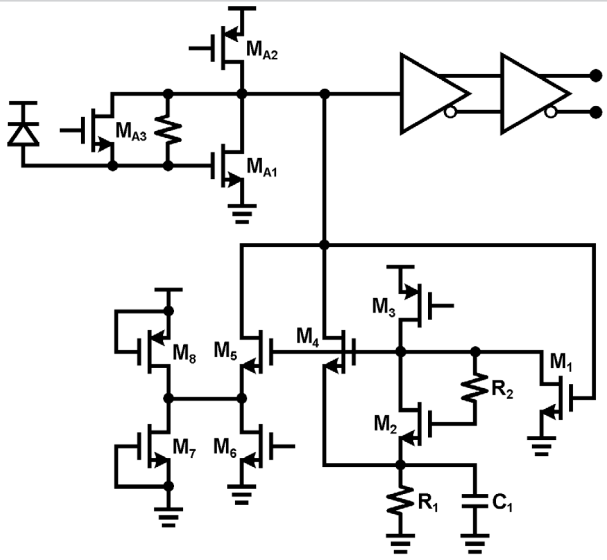

Figure 13.4.2: Complete circuit diagram of the TIA IC.

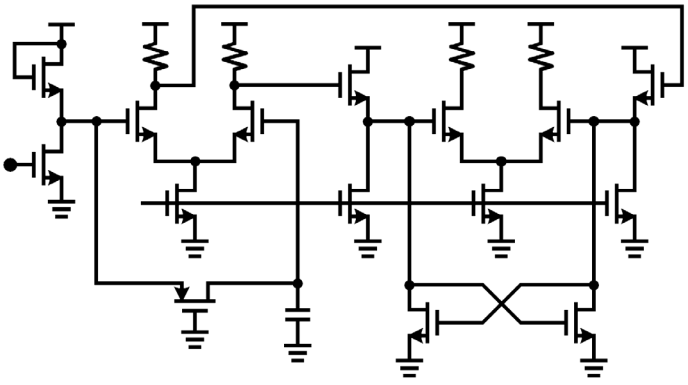

Figure 13.4.3: Schematic of the single-to-differential converter and the CML output buffer.

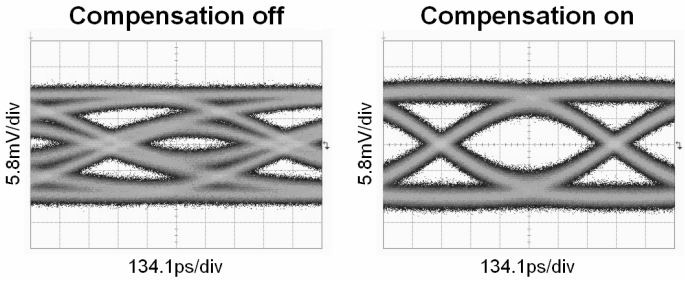

Figure 13.4.4: Measured 1.25Gb/s optical eye diagrams at -27dBm.

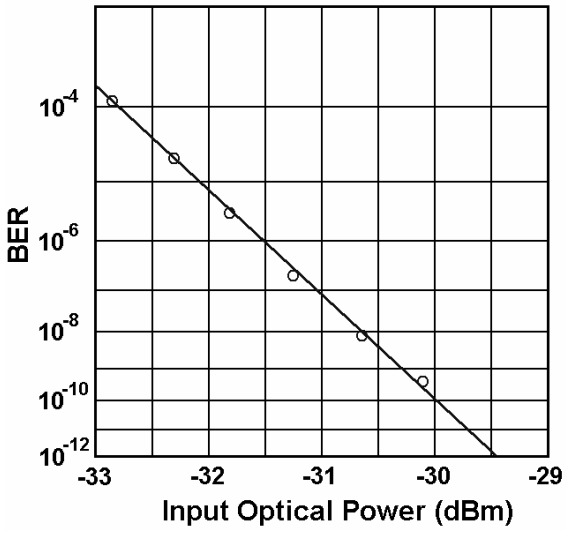

Figure 13.4.5: Measured BER versus input optical power at 1.25Gb/s.

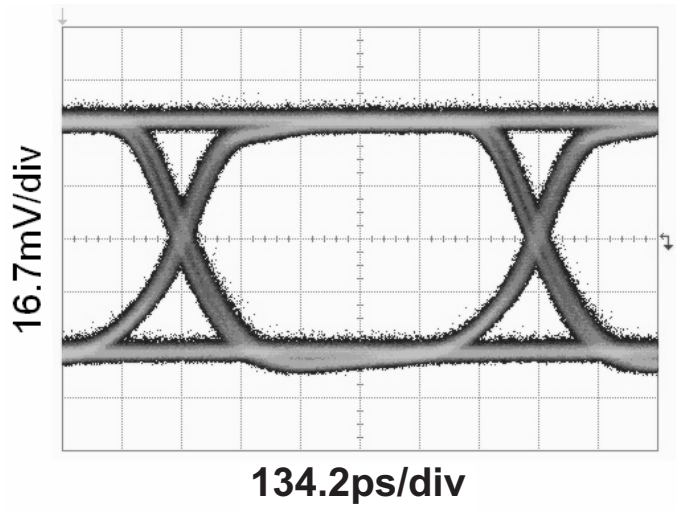

Figure 13.4.6: Measured 1.25Gb/s optical eye diagram at 0dBm.

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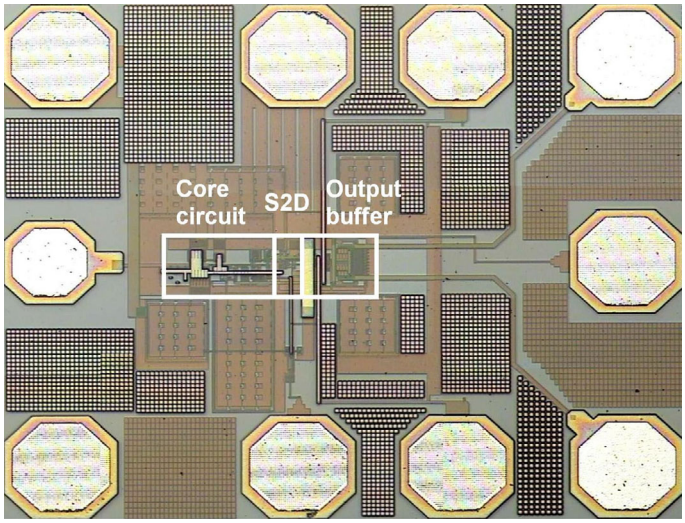

Figure 13.4.7: Die micrograph.

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